

WHAT IS CLAIMED IS:

5 1. A semiconductor chip package, comprising:
a substrate having a plurality of terminals;
a semiconductor chip on said substrate, said semiconductor chip including,
a plurality of inner bond pads,
a first insulation layer covering said chip,
a first plurality of holes in said first insulation layer exposing said inner
bond pads,
a metal layer disposed over said first insulation layer in contact with said
10 inner bond pads,
a second insulation layer disposed over said metal layer, and
a second plurality of holes in said second insulation layer exposing selected
portions of said metal layer to form external connection points; and
15 electrically conductive epoxy disposed between said external connection points of
said semiconductor chip and said terminals of said substrate, thereby electrically
connecting said semiconductor chip to said substrate.

2. A semiconductor chip package as in Claim 1, wherein said substrate is a
printed circuit board.

3. A semiconductor chip package as in Claim 1, wherein said semiconductor chip is disposed on said substrate face-down such that said external connection points are positioned directly above said terminals on said substrate.

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4. A semiconductor chip package as in Claim 2, wherein said semiconductor chip includes four edges and said external contact points are located on said semiconductor chip internally from said edges.

5. A semiconductor chip package as in Claim 1, wherein said semiconductor chip is disposed on said substrate face-up such that said external connection points face-away from said terminals on said substrate.

6. A semiconductor chip package as in Claim 5, wherein said semiconductor chip includes four edges and said external contact points are located along the edges of said semiconductor chip.

7. A semiconductor chip package as in Claim 6, wherein said semiconductor chip includes beveled edge walls and said electrically conductive epoxy extends down from said external contact points along said beveled edge walls to said terminals on said substrate.

8. A method for producing a multichip package, said method

comprising the steps of:

providing inner bond pads on said chip;

covering said chip with a first insulation layer;

5 forming a first plurality of holes in said first insulation layer to expose said inner bond pads;

disposing a metal layer over said first insulation layer such that said metal layer is in contact with said inner bond pads;

disposing a second insulation layer over said metal layer;

10 exposing selected portions of said metal layer to form external connection points;

providing a substrate having a plurality of terminals; and

disposing conductive epoxy between said external connection points of said chip and said terminals of said substrate to electrically connect said chip to said substrate.

9. A method as in Claim 8, further comprising the step of disposing

said chip is on said substrate face-down such that said external connection points are

positioned directly above said terminals on said substrate.

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A method as in Claim 9, further comprising the steps of:

providing said chip with four edges; and

forming said external contact points on said chip internally from said edges.

11. A method as in Claim 8, further comprising the step of disposing said substrate face-up on said substrate such that said external connection points face-away from said terminals on said substrate.

¹⁵/₁₂. A method as in Claim ¹⁴/₁₁, further comprising the steps of:
providing said chip with four edges; and
forming said external contact points along the edges of said chip.

¹⁶/₁₃. A method as in Claim ¹⁵/₁₂, further comprising the steps of:
providing said chip with beveled edge walls; and dispensing said electrically
conductive epoxy from said external contact points along said beveled edge walls to said
terminals on said substrate.

14. A flip-chip package, comprising:

a printed circuit board having a plurality of terminals;

a flip-chip including,

four edges;

a plurality of inner bond pads,

a first insulation layer covering said flip-chip,

a first plurality of holes in said first insulation layer exposing said inner bond pads,

a metal layer disposed over said first insulation layer in contact with said inner bond pads

a second insulation layer disposed over said metal layer, and

a second plurality of holes in said second insulation layer exposing selected portions of said metal layer to form external connection points, said external connection points being located on said flip-chip internally from said edges;

said flip-chip disposed on said printed circuit board face-down such that said external connection points are positioned directly above said terminals on said printed circuit board; and

electrically conductive epoxy disposed between said external connection points of said flip-chip and said terminals of said printed circuit board, thereby electrically connecting said chip to said printed circuit board.

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15. A chip package, comprising:

a printed circuit board having a plurality of terminals;

a chip including,

four edges;

a plurality of inner bond pads,

a first insulation layer covering said chip,

a first plurality of holes in said first insulation layer exposing said inner bond pads,

a metal layer disposed over said first insulation layer in contact with said inner bond pads

a second insulation layer disposed over said metal layer,

a second plurality of holes in said second insulation layer exposing selected portions of said metal layer to form external connection points, said external connection points being located along said edges of said chip, and

beveled edge walls;

said chip disposed on said printed circuit board face-up; and electrically conductive epoxy disposed along said beveled edge walls between said external contact points of said chip and said terminals of said printed circuit board, thereby electrically connecting said chip to said printed circuit board.

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